WHAT IS CLAIMED IS:

1. A semiconductor device comprising an element forming region where wiring is specified with the boundary on the main surface of a semiconductor substrate and a dummy region where wiring adjacent to said boundary is not formed, wherein said dummy region has at least two dummy pattern groups, a plurality of conductive islands formed with the conductive layer same as said wiring of the same shape and same size occupying the surface are placed, in each dummy pattern group, in isolation in both row and column directions with the insulation film, and the sizes of a plurality of said conductive islands in the row and/or column direction are different among the dummy pattern groups.

2. A method of manufacturing a semiconductor device where an element forming region in which circuit elements are formed and a dummy region in which circuit elements are not formed are specified with the boundary and at least two dummy pattern groups are formed in said dummy region, comprising the steps of:

(a) forming, on the main surface of the semiconductor substrate, the first isolation groove for specifying the active region of said element forming region and the second isolation groove for dividing a plurality of semiconductor islands forming a dummy pattern group in both row and column directions;

(b) depositing an insulation film covering said element forming region and said dummy region in such a manner as embedding said first isolation groove and said second isolation groove; and

(c) removing the external insulation film of said first isolation groove and second isolation groove by polishing said insulation film,

whereby a plurality of semiconductor islands of the same shape and the same size occupying the surface are formed in each dummy pattern group but sizes of a plurality of said semiconductor islands in the row direction and/or column direction are different among the dummy pattern groups.

3. A method of manufacturing a semiconductor element according to claim 2, further comprising the process to form a resist pattern covering the relatively wide isolation groove prior to said process (c) and to etch the upper part of said insulation film not covered with said resist pattern.

4. A method of manufacturing a semiconductor device according to claim 3, wherein when the sizes in the row and/or column direction of a plurality of semiconductor islands forming a first dummy pattern group among said dummy pattern groups are smallest, the size identical to the size of a side of one semiconductor island among said first dummy pattern group + space size is specified to the 1/integer of the size identical to the size of a side of one semiconductor island in another pattern group + space size among adjacent semiconductor islands in both row and column directions.

5. A method of manufacturing a semiconductor device according to claim 3, wherein a silicon oxide film, a silicon nitride film are sequentially formed from the lower layer under said insulation film and said silicon nitride film functions as a stopper layer in the process to polish said insulation film.

6. A method of manufacturing a semiconductor device according to claim 2, wherein when the sizes in the row and/or column direction of a plurality of semiconductor islands forming a first dummy pattern group among said dummy pattern groups are smallest, the size identical to the size of a side of one semiconductor island among said first dummy pattern group + space size is specified to the 1/integer of the size identical to the size of a side of one semiconductor island in another pattern group + space size among adjacent semiconductor islands in both row and column directions.

7. A method of manufacturing a semiconductor device according to claim 2, wherein a silicon oxide film, a silicon nitride film are sequentially formed from the lower layer under said insulation film and said silicon nitride film functions as a stopper layer in the process to polish said insulation film.

8. A method of manufacturing a semiconductor device where an element forming region in which circuit elements are formed and a dummy region in which circuit elements are not formed are specified with the boundary and at least two dummy pattern groups are formed in said dummy region, comprising the steps of:

(a) forming the first isolation groove for specifying an active region of said element forming region on the main surface of a semiconductor substrate and the second isolation groove for dividing a plurality of semiconductor islands forming said each dummy pattern group of said dummy region in both row and column directions;

(b) depositing an insulation film covering said element forming region and said dummy region in such a manner as embedding said first isolation groove and second isolation groove and thereafter depositing the coated insulation film at the upper layer of said insulation film;

(c) removing said coated insulation film with the etch-back method and moreover flattening the surface of said insulation film; and

(d) removing said insulation film in the external side of said first isolation groove and said second isolation groove by polishing said insulation film;

whereby a plurality of semiconductor islands of the same shape and the same size occupying the surface are formed in each dummy pattern group but sizes of a plurality of said semiconductor islands in the row direction and/or column direction are different among the dummy pattern groups.

9. A method of manufacturing a semiconductor device according to claim 8,

wherein when the sizes in the row and/or column direction of a plurality of semiconductor islands forming a first dummy pattern group among said dummy pattern groups are smallest, the size identical to the size of a side of one semiconductor island among said first dummy pattern group + space size is specified to the 1/integer of the size identical to the size of a side of one semiconductor island in another pattern group + space size among adjacent semiconductor islands in both row and column directions.

10. A method of manufacturing a semiconductor device according to claim 8,

wherein a silicon oxide film, a silicon nitride film are sequentially formed from the lower layer under said insulation film and said silicon nitride film functions as a stopper layer in the process to polish said insulation film.

11. A method of manufacturing a semiconductor device where an element forming region in which circuit elements are formed and a dummy region in which circuit elements are not formed are specified with the boundary and at least two dummy pattern groups are formed in said dummy region, comprising the processes of:

(a) depositing the first insulation film, the first silicon film and the second insulation film forming a gate insulation film on the semiconductor substrate;

(b) forming the first isolation groove for specifying an active region of said element forming region and the second isolation groove for dividing a plurality of semiconductor islands forming said each dummy pattern group of said dummy region by etching said second insulation film, said first silicon film, said first insulation film and said semiconductor substrate;

(c) depositing the third insulation film covering said element forming region and said dummy region in such a manner as embedding said first isolation groove and said second isolation groove;

(d) removing said third insulation film at the external side of said first isolation groove and said second isolation groove by polishing said third insulation film;

(e) depositing the second silicon film on said semiconductor substrate after removing said second insulation film; and

(f) forming a gate electrode by processing said second silicon film and said first silicon film;

whereby a plurality of semiconductor islands of the same shape and the same size occupying the surface are formed in each dummy pattern group but sizes of a plurality of said semiconductor islands in the row direction and/or column direction are different among the dummy pattern groups.

12. A method of manufacturing a semiconductor device according to claim 11, wherein when the sizes in the row and/or column direction of a plurality of semiconductor islands forming a first dummy pattern group among said dummy pattern groups are smallest, the size identical to the size of a side of one semiconductor island among said first dummy pattern group + space size is specified to the 1/integer of the size identical to the size of a side of one semiconductor island in another pattern group + space size among adjacent semiconductor islands in both row and column directions.

13. A method of manufacturing a semiconductor device according to claim 11, wherein said second insulation film is formed of a silicon nitride film, while said second insulation film functions as a stopper layer in the process to polish said third insulation film.

14. A method of manufacturing a semiconductor element where an element forming region in which wiring is formed and a dummy region in which wiring is not formed are specified with the boundary and at least two dummy pattern groups are formed in said dummy region, comprising the processes of:

(a) forming wiring in said element forming region by patterning the conductive film deposited on a semiconductor substrate and then forming a plurality of conductive islands placed in the row and column directions to form each dummy pattern group in said dummy region;

(b) depositing an insulation film covering said wiring and a plurality of said conductive islands; and

(c) flattening the surface of said insulation film,

whereby a plurality of semiconductor islands of the same shape and the same size occupying the surface are formed in each dummy pattern group but sizes of a plurality of said semiconductor islands in the row direction and/or column direction are different among the dummy pattern groups.

15. A method of manufacturing a semiconductor device according to claim 14,

wherein when the size in the row and/or column direction of a plurality of conductive islands forming a first dummy pattern group among said dummy pattern groups is smallest, the size identical to the size of a side of one conductive island in said first dummy pattern group + the space size among adjacent conductive islands is specified to 1/integer of the size identical to the size in both row and column directions of a side of one conductive island in another dummy pattern group + the space size among the adjacent conductive islands.

16. A method of designing a semiconductor device, where an element forming region on the main surface of a semiconductor substrate in which circuit elements are specified with the boundary and a dummy region in which circuit elements adjacent to said boundary are not formed are comprised, said dummy region includes at least two dummy pattern groups, a plurality of patterns of the same shape and same size occupying the surface are placed in isolation in the row and column directions in each dummy pattern group, and the sizes in the row and column directions of a plurality of said patterns are different among the dummy pattern groups, comprising the process of:

placing a plurality of patterns for said each dummy pattern group after said element forming region and said dummy region are specified with the boundary;

whereby a mesh in the size identical to the size of a side of a pattern forming a dummy pattern group + the space size among the adjacent patterns is generated for each dummy pattern group and a pattern is placed within said mesh in the region other than the pattern placement prohibiting region.

17. A method of designing a semiconductor device according to claim 16, wherein when the size in the row and/or column direction of a plurality of patterns forming a first dummy pattern group among said dummy pattern groups is smallest, the size identical to the size of a side of one pattern in said first dummy pattern group + the space size among adjacent patterns is specified to 1/integer of the size identical to the size in both row and column directions of a side of one pattern in another dummy pattern group + the space size among the adjacent patterns.

18. A method of designing a semiconductor device according to claim 17, wherein the space size in the row direction among the adjacent patterns is identical among said dummy pattern groups and the space size in the column direction among the adjacent patterns is identical among said dummy pattern groups.

19. A method of designing a semiconductor device according to claim 16, wherein the space size in the row direction among the adjacent patterns is identical among said dummy pattern groups and the space size in the column direction among the adjacent patterns is identical among said dummy pattern groups.

20. A method of designing a semiconductor device according to claim 17, wherein the shape of a plurality of said patterns is the square or rectangular shape.

21. A method of designing a semiconductor device according to claim 16, wherein the shape of a plurality of said patterns is the square or rectangular shape.